BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,144	12/20/2001	Patrice Roussel	10559-644001 / P12488	3547

20985 7590 06/23/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,144	ROUSSEL, PATRICE	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic, must all be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 59-72 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Referring to claims 59, 63, and 68, the limitation: "A hardware-based multithreaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; context event switching logic;" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the

inventor(s), at the time the application was filed, had possession of the claimed invention. Appropriate correction is required.

5. Claims 59-72 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Referring to claims 59, 63, and 68, the limitation: "A hardware-based multithreaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; context event switching logic;" was not enabled by the specification to one of ordinary skill in the art at the time the invention was made without undue experimentation. Appropriate correction is required.

6. Claims 60-62, 64-67, and 69-72 are rejecting for incorporating the defects of the claims from which they depend. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 5, 9, and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sidwell et al., European Patent Application EP 0 743 594 A1, cited on the information disclosure statement filed on June 9, 2003.

9. Referring to claim 1, Sidwell et al. have taught a computer instruction comprises:

a. a move and duplicate instruction that causes a processor to load a first portion of bits of a source into a first portion of a destination register and duplicate that first portion of bits in a subsequent portion of the destination register (Figure 6, page 5, line 44-page 6, line 14).

10. Referring to claim 5, Sidwell et al. have taught a method comprising:

a. in a processor, loading a first portion of bits of a source into a first portion of a destination register; and duplicating the first portion of bits in a subsequent portion of the destination register (Figure 6, page 5, line 44-page 6, line 14).

11. Referring to claim 9, Sidwell et al. have taught a computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

a. load a first portion of bits of a source into a first portion of a destination register (Figure 6, page 5, line 44-page 6, line 14); and

b. duplicate the first portion of bits in a subsequent portion of the destination register (Figure 6, page 5, line 44-page 6, line 14).

12. Referring to claim 19, Sidwell et al. have taught a method executed in a processor comprising:

a. loading a first number N of bits from a source into a lower half of a 2N wide-bit destination register and in a upper half of the 2N-bit wide destination register (Figure 6, page 5, line 44-page 6, line 14).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 2-4, 6-8, 10-18, 20-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell et al., European Patent Application EP 0 743 594 A1, cited on the information disclosure statement filed on June 9, 2003.

15. Referring to claim 2, Sidwell et al. have taught the instruction of claim 1, as described above, and wherein the first portion of the source is in a memory location (Figure 6, element 104). Sidwell et al. have not have specifically taught in which the first portion of the source is 64-bits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first portion of the source of Sidwell et al. be 64-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

16. Furthermore Sidwell et al. have not taught the first portion of the source represents a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The move and duplicate instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

17. Referring to claim 3, Sidwell et al. have taught the instruction of claim 1, as described above, and in which the first portion of the source is in a source register (Figure 6, element 104). Sidwell et al. have not specifically taught in which the first portion of the source is 64-bits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first portion of the source of Sidwell et al. be 64-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

18. Furthermore Sidwell et al. have not taught in which the first portion of the source represents a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The move and duplicate instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

19. Referring to claim 4, Sidwell et al. have taught the instruction of claim 1 as described above. Sidwell et al. have not specifically taught in which the first portion of the destination register is loaded with bits [63-0] of the first portion of the source and the subsequent portion of the destination register is loaded with bits [63-0] of the first portion of the source. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first portion of the destination register is loaded with bits [63-0] of the first portion of the source and the subsequent portion of the destination register is loaded with bits [63-0] of the first

portion of the source, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

20. Claims 6, 10, 20, and 21 do not recite limitations above the claimed invention set forth in claim 2 and are therefore rejected for the same reasons set forth in the rejection of claim 2 above.

21. Claims 7 and 11 do not recite limitations above the claimed invention set forth in claim 3 and are therefore rejected for the same reasons set forth in the rejection of claim 3 above.

22. Claims 8 and 12 do not recite limitations above the claimed invention set forth in claim 4 and are therefore rejected for the same reasons set forth in the rejection of claim 4 above.

23. Claim 6 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

24. Claim 7 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

25. Claim 8 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

26. Referring to claim 13, Sidwell et al. have taught a computer instruction comprises:

a. a move and duplicate instruction that causes a processor to load bits of a source and return the bits in a lower half of a destination and a upper half of a destination (Figures 6 and 17, page 5, line 44-page 6, line 14).

27. Sidwell et al. have not specifically taught that the move and duplicate instruction is for manipulating double floating point data. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The move and duplicate instruction would be performed the same regardless of the data. Thus this

descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

28. Furthermore, Sidwell et al. have not taught that the number of bits is 64. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the number of bits be 64-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

29. Referring to claim 14, Sidwell et al. have taught the instruction of claim 13, as described above, and further comprising: a source operand (Figure 6, page 5, line 44-page 6, line 14, element 104); and a destination operand (Figure 6, page 5, line 44-page 6, line 14, element 112). Referring to claim 15, Sidwell et al. have taught the instruction of claim 13, as described above, and in which the source operand is a memory location (Figure 6, page 5, line 44-page 6, line 14, element 104).

30. Referring to claim 16, Sidwell et al. have taught the instruction of claim 15, as described above. Sidwell et al. have not specifically taught in which the memory location has a 128-bit value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the memory location have a 128-bit value, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

31. Furthermore, Sidwell et al. have not taught in which the memory location bit value represents a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The

move and duplicate instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

32. Referring to claim 17, Sidwell et al. have taught the instruction of claim 13, as described above, and wherein the source operand is in a register (Figure 6, element 104). Sidwell et al. have not specifically taught in which the source operand is a 128-bit source register. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source register be 128-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

33. Referring to claim 18, Sidwell et al. have taught the instruction of claim 17, as described above. Sidwell et al. have not specifically taguth in which the source register has a 128-bit value that represents a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The move and duplicate instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

34. Referring to claim 22, Sidwell et al. have taught the method of claim 19, as described above, and in which the source is a 128-bit source register and N is 64 bits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source

register and N be any number of bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

35. Referring to claim 23, Sidwell et al. have taught the method of claim 19, as described above, and in which the 128-bit source register contains a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The move and duplicate instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

36. Referring to claim 24, Sidwell et al. have taught a computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to: load bits from a source in a lower half of a destination register and in an upper half of the destination register. Sdiwell et al. have not specifically taught loading 64-bits from a source in a lower half of a 128-bit destination register and in an upper half of the 128-bit destination register. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have load any number of bits from a source into any bit sized destination register, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

37. Referring to claim 25, Sidwell et al. have taught the computer program product of claim 24, as described above, and wherein the source is a memory location (Figure 6, element 104). Sidwell et al. have not taught in which the source is 128-bits. It would have been obvious to one

of ordinary skill in the art at the time the invention was made to have the source be any number of bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

38. Furthermore, Sidwell et al. have not specifically taught in which the source is a floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

39. Referring to claim 26, Sidwell et al. have taught the computer program product of claim 24, as described above, and in which the source is a source register (Figure 6, element 104). Sidwell et al. have not taught in which the source is a 128-bits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source be any number of bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955). Furthermore, Sidwell et al. have not taught in which the source is a double floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

40. Referring to claim 27, Sidwell et al. have taught a computer instruction comprises:

a. a move packed single floating point high and duplicate instruction that causes a processor to load bits of a source and return bits of the source in bits of a 128-bit destination register, bits of the source in bits of the destination register, bits of the source in bits of the destination register and bits of the source in bits of the destination register (Figures 6 and 17, page 5, line 44-page 6, line 14).

41. Sidwell et al. have not taught a move high and duplicate instruction that causes a processor to load bits [127-0] of a source and return bits [63-32] of the source in bits [31-0] of a 128-bit destination register, bits [63-32] of the source in bits [63-32] of the destination register, bits [127-96] of the source in bits [95-64] of the destination register and bits [127-96] of the source in bits [127-96] of the destination register. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Sidwell et al. load any number of bits to and from any location as it has been held that a change in size is not a patentable difference, see In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955), and that shifting the location of parts is not a patentable difference, see In re Japikse, 181 F.2d 1019, 1023, 86 USPQ70, 73 (CCPA 1950).

42. Furthermore, Sidwell et al. have not specifically taught that the move and duplicate instruction is intended for packed single floating point data. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

43. Claims 28-32 do not recite limitations above the claimed invention set forth in claims 14-18, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 14-18 above.

44. Referring to claim 33, Sidwell et al. have taught a method executed in a processor comprising: accessing bits of a source; and returning bits of the source in bits of the destination register; and bits of the source in bits of the destination register (Figures 6 and 17, page 5, line 44-page 6, line 14). Sidwell has not specifically taught accessing bits [127-0] of a source; and returning bits [63-32] of the source in bits [31-0] and bits [63-32] of the destination register; and bits [127-96] of the source in bits [95-64] and bits [127-96] of the destination register. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Sidwell et al. load any number of bits to and from any location as it has been held that a change in size is not a patentable difference, see In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955), and that shifting the location of parts is not a patentable difference, see In re Japikse, 181 F.2d 1019, 1023, 86 USPQ70, 73 (CCPA 1950).

45. Referring to claim 34, Sidwell et al. have taught the method of claim 33, as described above, and in which the source is a memory location (Figure 6, page 5, line 44-page 6, line 14, element 104).

46. Referring to claim 35, Sidwell et al. have taught the method of claim 34, as described above. Sidwell et al. have not specifically taught in which the memory location contains a packed single floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The instruction would be performed the same regardless of the data. Thus this descriptive material

will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

47. Referring to claim 36, Sidwell et al. have taught the method of claim 33, as described above, in which the source is a source register (Figure 6, element 104). Sidwell et al. have not specifically taught in which the source is a 128-bits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source of Sidwell et al. be any number of bits, since it has been held that a change in size is not a patentable difference, see In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955), and that shifting the location of parts is not a patentable difference, see In re Japikse, 181 F.2d 1019, 1023, 86 USPQ70, 73 (CCPA 1950).

48. Referring to claim 37, Sidwell et al. have taught the method of claim 36, as described above. Sidwell et al. have not specifically taught in which the 128-bit source register contains a packed single floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The instruction would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

49. Claims 38-42 do not recite limitations above the claimed invention set forth in claims 33-37, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 33-37 above.

50. Referring to claim 43, Sidwell et al. have taught a computer instruction comprises:

a. a move a packed single floating point low and duplicate instruction that causes a processor to load bits of a source and return bits of the source in bits of a 128-bit destination register, bits of the source in bits of the destination register, bits of the source in bits of the destination register and bits of the source in bits of the destination register (Figures 6 and 17, page 5, line 44-page 6, line 14).

51. Sidwell et al. have not specifically taught a move a packed single floating point low and duplicate instruction that causes a processor to load bits [127-0] of a source and return bits [31-0] of the source in bits [31-0] of a 128-bit destination register, bits [31-0] of the source in bits [63-32] of the destination register, bits [95-64] of the source in bits [95-64] of the destination register and bits [95-64] of the source in bits [127-96] of the destination register. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Sidwell et al. load any number of bits to and from any location as it has been held that a change in size is not a patentable difference, see In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955), and that shifting the location of parts is not a patentable difference, see In re Japikse, 181 F.2d 1019, 1023, 86 USPQ70, 73 (CCPA 1950).

52. Referring to claim 44, Sidwell et al. have taught the instruction of claim 43, as described above, and further comprising: a source address field (Figures 6 and 17, page 5, line 44-page 6, line 14, element 104); and the destination register (Figures 6 and 17, page 5, line 44-page 6, line 14, element 112).

53. Referring to claim 45, Sidwell et al. have taught the instruction of claim 44, as described above, and in which the source is a memory location (Figures 6 and 17, page 5, line 44-page 6, line 14, element 104).

54. Claim 46 does not recite limitations above the claimed invention set forth in claim 37 and is therefore rejected for the same reasons set forth in the rejection of claim 37 above.

55. Claim 47 does not recite limitations above the claimed invention set forth in claim 36 and is therefore rejected for the same reasons set forth in the rejection of claim 36 above.

56. Claim 48 does not recite limitations above the claimed invention set forth in claim 37 and is therefore rejected for the same reasons set forth in the rejection of claim 37 above.

57. Claim 49 does not recite limitations above the claimed invention set forth in claim 43 and is therefore rejected for the same reasons set forth in the rejection of claim 43 above.

58. Claim 50 does not recite limitations above the claimed invention set forth in claim 45 and is therefore rejected for the same reasons set forth in the rejection of claim 45 above.

59. Claim 51 does not recite limitations above the claimed invention set forth in claim 35 and is therefore rejected for the same reasons set forth in the rejection of claim 35 above.

60. Claim 52 does not recite limitations above the claimed invention set forth in claim 36 and is therefore rejected for the same reasons set forth in the rejection of claim 36 above.

61. Claim 53 does not recite limitations above the claimed invention set forth in claim 37 and is therefore rejected for the same reasons set forth in the rejection of claim 37 above.

62. Claim 54 does not recite limitations above the claimed invention set forth in claim 43 and is therefore rejected for the same reasons set forth in the rejection of claim 43 above.

63. Claim 55 does not recite limitations above the claimed invention set forth in claim 45 and is therefore rejected for the same reasons set forth in the rejection of claim 45 above.

64. Claim 56 does not recite limitations above the claimed invention set forth in claim 35 and is therefore rejected for the same reasons set forth in the rejection of claim 35 above.

65. Claim 57 does not recite limitations above the claimed invention set forth in claim 36 and is therefore rejected for the same reasons set forth in the rejection of claim 36 above.

66. Claim 58 does not recite limitations above the claimed invention set forth in claim 48 and is therefore rejected for the same reasons set forth in the rejection of claim 48 above.

67. Claims 59-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell et al., European Patent Application EP 0 743 594 A1, cited on the information disclosure statement filed on June 9, 2003, in view of Wolrich et al., US Patent 6,560,667.

68. Referring to claim 59, Sidwell et al. have taught a hardware-based processor comprising:

a. an execution box data path including an arithmetic logic unit (ALU) and a general purpose register set, the ALU performing functions in response to instructions, one of the instructions causing the ALU to load a first portion of bits of a source into a first portion of a destination register and duplicate that first portion of bits in a subsequent portion of the destination register (Figures 6 and 17, page 5, line 44-page 6, line 14).

69. Sidwell et al. have not specifically taught a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic. However, Wolrich et al. have taught a hardware-based multi-threaded processor comprising: a plurality of microengines (Figure 1, element 22), each of the microengines comprising: a control store (Figure 3A, element 70);

controller logic (Figure 3A, element 72); and context event switching logic (Figure 3A, element 74), for the desirable purpose of processing many concurrent events in parallel (Column 1, line 5-25, column 1, line 55-column 2, line 3, column 54-column 3, lines 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the processor of Sidwell et al. be implemented as a a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic, as taught by Wolrich et al., for the desirable purpose of processing many concurrent events in parallel (Column 1, line 5-25, column 1, line 55-column 2, line 3, column 54-column 3, lines 14).

70. Claims 60-62 do not recite limitations above the claimed invention set forth in claims 2-4, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 2-4 above.

71. Referring to claim 63, Sidwell et al. have taught a hardware-based processor comprising:

a. an execution box data path including an arithmetic logic unit (ALU) and a general purpose register set, the ALU performing functions in response to instructions, one of the instructions causing the ALU to load a first number N of bits from a source into a lower half of a 2N wide-bit destination register and in a upper half of the 2N-bit wide destination register (Figures 6 and 17, page 5, line 44-page 6, line 14). Sidwell et al. have not specifically taught a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic. However, Wolrich et al. have taught a hardware-based multi-threaded processor comprising: a plurality of microengines (Figure 1, element 22),

each of the microengines comprising: a control store (Figure 3A, element 70); controller logic (Figure 3A, element 72); and context event switching logic (Figure 3A, element 74), for the desirable purpose of processing many concurrent events in parallel (Column 1, line 5-25, column 1, line 55-column 2, line 3, column 54-column 3, lines 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the processor of Sidwell et al. be implemented as a a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic, as taught by Wolrich et al., for the desirable purpose of processing many concurrent events in parallel (Column 1, line 5-25, column 1, line 55-column 2, line 3, column 54-column 3, lines 14).

72. Claims 64, 65, 66 and 67 do not recite limitations above the claimed invention set forth in claims 2, 2, 22, and 23, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 2, 2, 22, and 23 above.

73. Referring to claim 68, Sidwell et al. have taught a hardware-based processor comprising:

a. an execution box data path including an arithmetic logic unit (ALU) and a general purpose register set, the ALU performing functions in response to instructions, one of the instructions causing the ALU to access bits of a source, return bits of the source in bits and bits of the destination register, and bits of the source in bits and bits of the destination register (Figures 6 and 17, page 5, line 44-page 6, line 14).

74. Sidwell et al. have not specifically taught an execution box data path including an arithmetic logic unit (ALU) and a general purpose register set, the ALU performing functions in response to instructions, one of the instructions causing the ALU to access bits [127-0] of a

source, return bits [127-32] of the source in bits [31-0] and bits [63-32] of the destination register, and bits [127-96] of the source in bits [95-64] and bits [127-96] of the destination register. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Sidwell et al. access and return any number of bits to and from any location as it has been held that a change in size is not a patentable difference, see In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955), and that shifting the location of parts is not a patentable difference, see In re Japikse, 181 F.2d 1019, 1023, 86 USPQ70, 73 (CCPA 1950).

75. Furthermore, Sidwell et al. have not specifically taught a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic. However, Wolrich et al. have taught a hardware-based multi-threaded processor comprising: a plurality of microengines (Figure 1, element 22), each of the microengines comprising: a control store (Figure 3A, element 70); controller logic (Figure 3A, element 72); and context event switching logic (Figure 3A, element 74), for the desirable purpose of processing many concurrent events in parallel (Column 1, line 5-25, column 1, line 55-column 2, line 3, column 54-column 3, lines 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the processor of Sidwell et al. be implemented as a a hardware-based multi-threaded processor comprising: a plurality of microengines, each of the microengines comprising: a control store; controller logic; and context event switching logic, as taught by Wolrich et al., for the desirable purpose of processing many concurrent events in parallel (Column 1, line 5-25, column 1, line 55-column 2, line 3, column 54-column 3, lines 14).

76. Claims 69-72 do not recite limitations above the claimed invention set forth in claims 34-37, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 34-37 above.

Conclusion

77. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

78. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

79. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100